A Unique System Approach to Deliver Best FPGA/SoC Paired With Validated and Optimized Power Solutions

Arrow Vision Presentation

Jul 18th, 2013 rev 1.6





Agenda

- Introduction Altera acquisition
- Enpirion power products and technology
- FPGA power challenges
- PowerSoC benefits
- Reference design: 4 validated solutions



FPGA + Power : One Company, One Solution

Altera to Deliver Breakthrough Power Solutions for FPGAs with Acquisition of Power Technology Innovator Enpirion

Industry's Most Integrated Power Solutions Reduce Power, Provide Smallest Form Factor

and Simplify System Design

San Jose, Calif., May 14, 2013—Altera Corporation (NASDAQ: ALTR) today announced it has signed a definitive merger agreement to acquire Enpirion, Inc., the industry's leading provider of high-efficiency, integrated power conversion products known as PowerSoCs (power system-on-chip). The combination of Altera's FPGAs with Enpirion's PowerSoCs will offer customers higher performance, lower system power, higher reliability, smaller footprint and faster time-to-market.

"Power is increasingly a strategic choice for product differentiation in communications, computing and enterprise, and industrial applications," said John Daane, president, CEO and chairman of Altera. "By adding a power group to Altera, we will bring even more value to system-level designs. Altera's FPGA roadmap will be enhanced significantly with the addition of Enpirion's power technologies."

Ashraf Sounder an CEO of Envirion will see a Fellow chief

Acquisition completed May 21st 2013



Why Acquire a Power Company?

- FPGA power requirements are getting more complex
 - Number of rails, tolerances, load requirements, power up sequencing and layout
- Power is becoming a strategic differentiator for FPGA customers

 Adding power allows Altera to optimize system-level FPGA solutions





Who Is Enpirion?

- Founded in 2001 by Bell Labs experts
- Industry's most advanced PowerSoCs
- More than 60 released products
- 100 million units shipped
- Key Enpirion markets
 - Enterprise
 - Communications
 - Industrial
 - Test & Measurement















Enpirion PowerSoC Leadership in Integrated Power Conversion

High Efficiency + Low Noise

- Up to 96% efficiency with low ripple
- Lower system power

Increased System Reliability

- Fully simulated, characterized, and validated power system
- Fewer components



Ease-of-Use; Faster Time-to-Market

- Simple design flow with fewer iterations
- Lower development costs

Smallest Footprint



Enpirion PowerSoC, a Key Brand within Altera



POWERING YOUR INNOVATION







FPGAs





CPLDs
Lowest Cost,
Lowest Power

FPGAs

Cost/Power Balance Mid-range FPGAs SoC & Transceivers

FPGAs

Optimized for High Bandwidth

PowerSoCs
High-efficiency
Power Management

RESOURCES

Embedded Soft and Hard Processors

Nios'II

ARM



Development Kits



Intellectual Property (IP)

- Industrial
- Computing]
- Enterprise



Enpirion PowerSoC: Target Customers / Applications

Customer challenges to solve

- Minimizing power loss
- Board space constraint
- Noise sensitivity
- Time-to-market pressures; fewer resources
- While improving Cost & Reliability!

PowerSoC Benefits

- High efficiency, smallest size
- Excellent noise/transient performance
- Simple, low risk power design
- > Highest reliability, fewest components



Power FETs
PWM Controller
Inductor
Compensation Circuit

Target Markets



Enterprise userver



Storage



Telecom



Test & Measurement



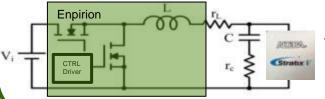
Embedded/ Industrial



Optical Networking

Target Specifications

- Step down conversion V_{IN}< V_{OUT}
- Input voltages: 3.3 V, 5 V, 12 V (V_{IN} <15 V)</p>
- Output voltage: 0.6 V to 6 V
- Output current: 300 mA to 15 A (60A in //)



Loads

- FPGA
- Digital Semi
- Memory
- *I/O*



Challenges For FPGA or Digital Semiconductor Power





Problem Statement

1. Limited space available on PCB

- PCB size is constrained due to industry standard form-factors while functionality increases (more ports, more memory, more functions on-board)
- Market forces require ever smaller product form-factor (Ex: cabinet→rack→card)

2. Enterprise, Industrial, Telco, Netcom markets demand higher reliability

- Solution assembled from multiple vendors and components not designed, qualified, tested as system.
- High part counts drive lower reliability and lower assembly yields
- Many power passives are high reliability risk such as electrolytic bulk capacitors

3. Customers need greater conversion efficiency

- Thermal limitations require less heat generation (conversion loss = heat);
- OPEX considerations drive lower cooling costs; poor efficiency = higher cooling costs

4. High-speed SERDES, RF circuits, PLLs, sensitive to noise

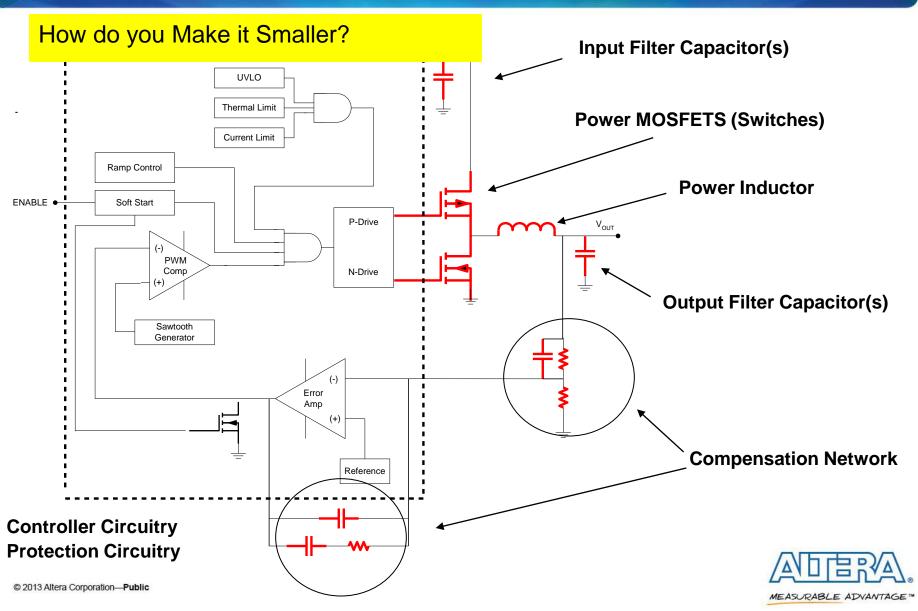
DC-DC converter noise can affect IO signal integrity, SERDES jitter, RF contamination

5. Limited design resource and fast time to market requirements

- Traditional power implementations require multiple design cycle iterations, multiple re-spins
- Power design is a highly specialized discipline; many customers have limited analog resources



Key Components of a Switch-Mode DC-DC Converter



Relationship Between Switch Frequency and Size

Inductor:

$$L = \frac{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{\Delta I_{OUT} F_{SWITCH}}$$

- Inversely proportional: higher the frequency, the smaller the inductor value
- Input Filter Capacitors

$$C_{IN} = \frac{D(1-D)}{\Delta V_{IN} F_{SWITCH}}$$
 where $\left[D = \frac{V_{OUT}}{V_{IN}}\right]$

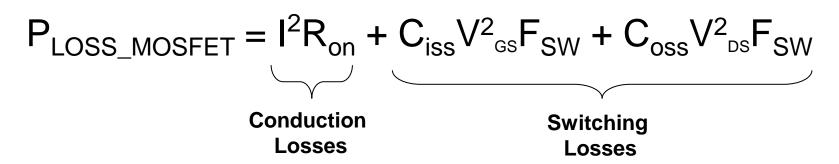
- Inversely proportional: higher the frequency, the smaller the capacitor value
- Output Filter Capacitors

$$C_{OUT_min} = \frac{\Delta I_{OUT}}{\Delta V_{OUT} F_{SWITCH}}$$

- Inversely proportional: higher the frequency, the smaller the capacitor value
- High Switch Frequency Allows Smaller Component Values
 Thereby Enabling PowerSoC Integration

However, Nothing Comes for Free!

While Higher Switching Frequency Enables Smaller Filter Component Values, It Increases Switch Losses:



R_{on} ---- On-Resistance

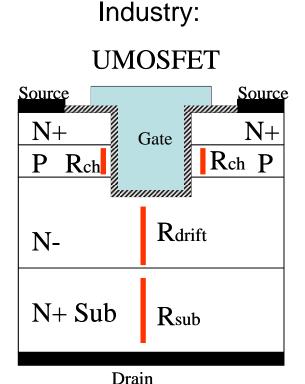
C_{iss} ---- FET Equivalent Input Capacitance

C_{oss} ---- FET Equivalent Output Capacitance

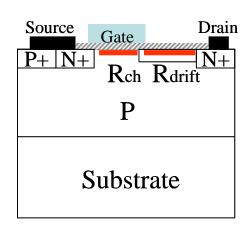


Enpirion Power MOSFET Design Reduces Switch Loss

Enpirion power MOSFET design reduces equivalent Input and Output capacitances by 10x so F_{SWITCH} can be 10x higher than competitors for similar switch loss



Enpirion: Small & High Performance

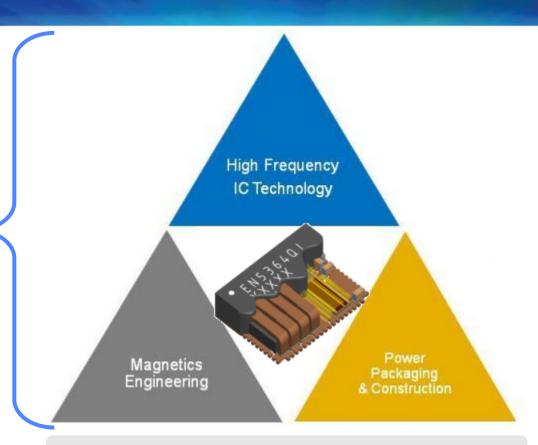


EDMOS



Key Enablers of High Density PowerSoC

3 Focused Technology
Development



DC-DC System Engineering

Inductor Selection Selection Compensation Design Stability Validation Testing Compensation Design Stability Production Testing



Powering Your Innovation

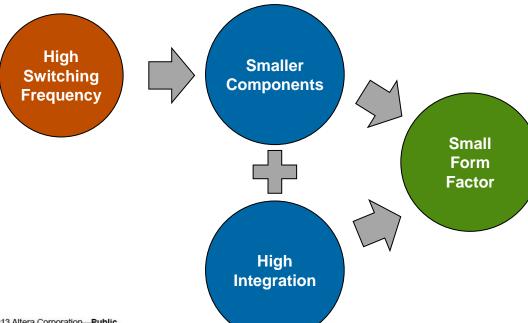
Reduced Form Factor

Inductor ——

Controller -

High Frequency Filter Caps

MOSFETS (2x)







Competitor A (Modules)



Competitor B (Discrete Regulators)



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Enpirion PowerSoC Product Benefits





Enpirion PowerSoCs Offer a Clear and Tangible Value Proposition

- Smallest Solution Size, Low Part Count
- High Efficiency, High Performance
- High Reliability; Typically 280,000 Years MTBF
- Low Noise Design; Low Ripple, Low EMI
- Ease of Design; Fast Design Cycle; First Pass Success
- Designed as a System, Qualified as a System, Tested as a System for Assured Reliability and Assured Performance



Enpirion PowerSoCs Deliver Highest Power Density

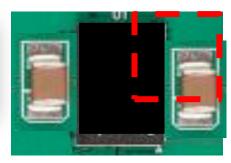
From 20% to 50% power density reduction

Enpirion PowerSoC

(Modules)

2X





20% lower height than the nearest module competitor

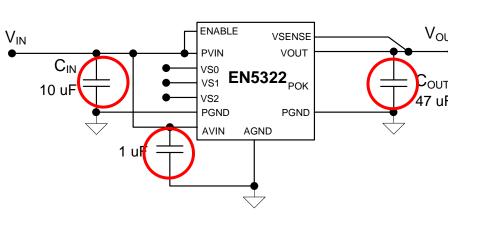
Comparison for 5V V_{IN}, 4A PowerSoC



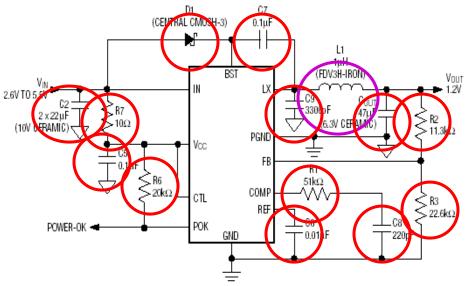
Value Proposition: Low Part Count

- Fewer placements means higher assembly yield
- Fewer components means higher reliability
- Enpirion requires ceramic Caps only; no POSCAP, OSCON
- Fewer components means lower BOM cost

Typical Part Count

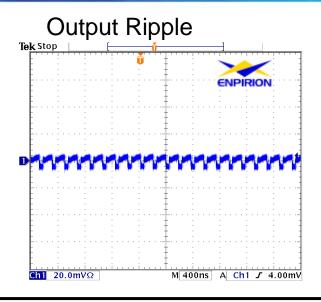


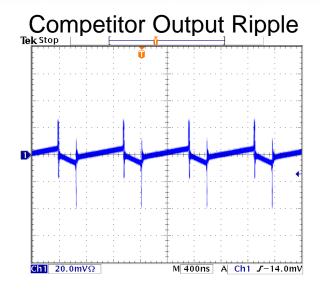
Competitor Typical Part Count



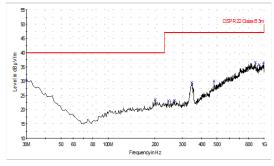


Value Proposition: Low Ripple, Low EMI



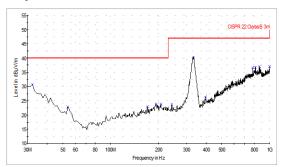


Radiated Emissions



4/27/10, MJO# 41632 - Enpirion Inc., EN6360QI, 5Vin, 1.5V out, 0.2 Ohm 30MHz - 1GHz Vertical Peak Scan (90 Degree Table Angles)

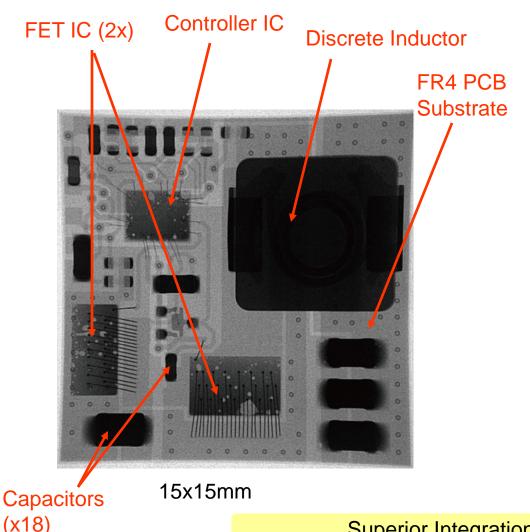
Competitor Radiated Emissions

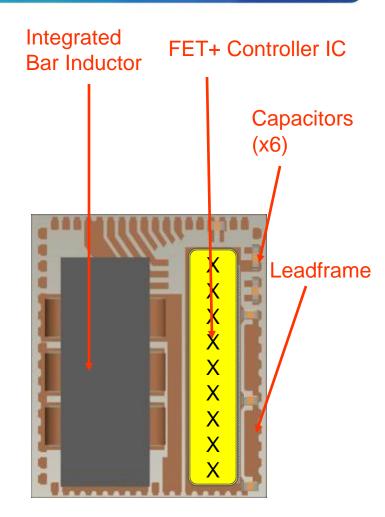


4/27/10, MJC# 41632 - Enpirion Inc., ISL8201M 5Vin, 1.5V out., 0.14 Ohm 30MHz - 1GHz. Vertical Peak Scan (90 Degree Table Angles)



Superior Integration vs. uModules







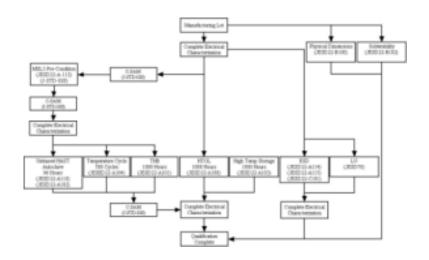


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Value Proposition: High Reliability

- Designed as a System, Qualified as a System, and Tested as a System!
- Device FIT rate = 0.4 (MTBF = 280,000 yrs)
 - @ 55°C, 1.0eV activation energy, 60% confidence level
- FIT Rate based on aggregate HTOL (High Temperature Operating Life) data

Item	Test	Standard	Test Condition
1	High Temperature Operating Life (HTOL)	JESD22-A108C	125°C, 5.5 to 15Vin, 1000 hours
2	Temperature Humidity Bias with Pre- Conditioning (Note 1)	JESD22-A101B	85°C, 85%RH, 5.5 to 15Vin, 1000 hours
3	Accelerated Moisture Resistance Unbiased HAST or Autoclave with Pre-conditioning (Note 1)	JESD22-A118B JESD22-A102C	85%RH, 130°C, 96 hours 100%RH, 121°C, 96 hours
4	Temperature Cycle with Pre-Conditioning (Note 1)	JESD22-A104C	–65°C to +150°C / 500 cycles Condition C, Soak Mode 4
5	High Temperature Storage (HTS)	JESD22-A103C	150°C, 1000 hours, Condition B
c	Electrostatic Discharge (ESD) – Human Body Model (HBM)	JESD22-A114E	2000V minimum Class 2
6	Electrostatic Discharge (ESD) – Field Induced Charge Device Model (CDM)	JESD22-C101C	500V minimum
7	Latch Up	JESD78A	Class I & II
8	Solderability	JESD22-B102D	Method 1; Lead-Free





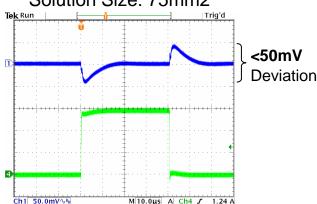
Value Proposition: Transient Performance

Enpirion PowerSoCs product have very high loop bandwidth

- Allow use of ceramic only capacitance (smaller size, cost and performance)
- Smaller output deviation meeting stringent max voltage requirement
- Voltage mode

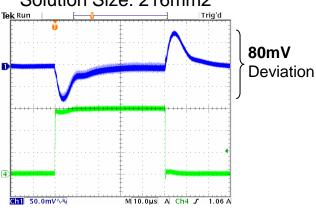
Enpirion: EN5337QI

Solution Size: 75mm2



Competitor

Solution Size: 216mm2

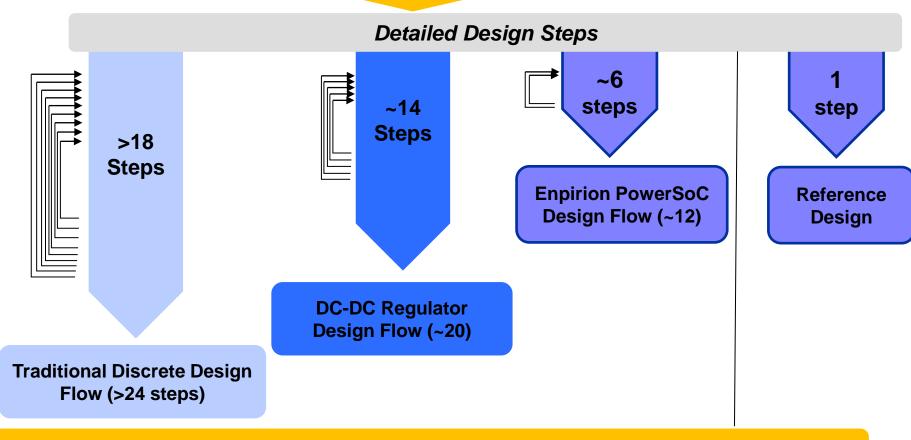


0 - 3A Slammer Load Transient



Ease of Design – 1 Step with Reference Designs

Common Pre-Design Steps (6)



Enpirion PowerSoC ~ 2X Faster Design Time & High Probability of 1st Pass Success



Altera Validated Solutions Simplify Design Process Reduce Risk, Effort, Time, Costs

Step 1

Run Altera Power Optimizer / Estimator

Step 2

Select Altera Validated PowerSoC

Step 3

 Use Validated FPGA Power Schematics / Gerbers / etc.

Faster Time-to-Market





Enpirion PowerSoC for LDO Replacement

- Customers tend to use LDO's to power noise sensitive transceiver supply rails due to their low noise characteristic, but, at the cost of power loss and thermal dissipation.
- Altera's Enpirion PowerSoCs provide the low noise and simple design of an LDO, but provide the high conversion efficiency of a switch-mode DCDC converter.
- To demonstrate this thesis, a Stratix V GX FPGA board was used to compare jitter and efficiency for a bench supply, a LDO regulator, and Altera's Enpirion PowerSoC
 - The jitter was essentially the same for all three supplies
 - The efficiency was 83% for the PowerSoC vs 30% for the LDO
- PowerSoC <u>CAN</u> supply sensitive SERDES rails with no jitter degradation and with a dramatic improvement in power loss



LDO Replacement for Transceiver Power

Brief Introduction to Power Conversion:

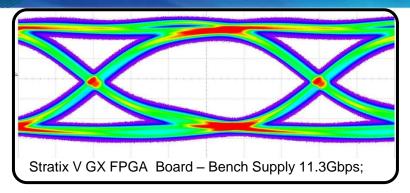
- Linear Regulator
 - Utilizes a resistive element and a feedback network to regulate voltage
 - Benefits: Small Solution, low part count, low noise, simple design
 - Drawbacks: low conversion efficiency, increased thermal dissipation
- Switch-mode DCDC Converter
 - Utilizes magnetic storage and a feedback network to regulate voltage
 - Benefits: High conversion efficiency, lower thermal dissipation
 - Drawbacks: larger solution size, noise source, complex design, more parts
- Altera's Enpirion PowerSoC
 - Benefits: High efficiency, low part count, low noise, low design complexity

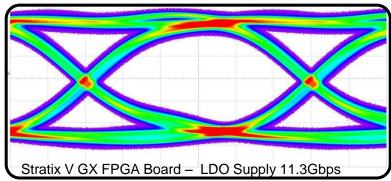
What is a PowerSoC?

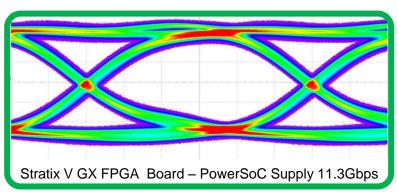
- A highly integrated switch-mode DCDC converter
 - Integrated controller, MOSFET switches, and Inductor in a single package
 - Integration reduces noise and simplifies design complexity.
 - Designed as a complete system, qualified as a complete system, and production time tested as a complete system, for high reliability and 95% first pass success



PowerSoC, Quiet and Efficient for SERDES







Configuration	Tj (ps)	Rj (fs)	Efficiency*
Bench Supply	19.55	682	-
LDO	19.89	685	30%
PowerSoC	19.32	681	83%

* VIN=3.3V, VOUT=1.0V

EN6337QI on VCCRT_GXB, VCCA_GXB



Reference Designs

Validated Solution Altera FPGA/SoC and Power





4 Reference Designs

Availability

- 4Q'13

Broad support for 28 nm portfolio

Cyclone V SoC



Cost Efficiency Space

Turn key design

Characterization data

Fully tested solutions

- Schematic
- Layout files

Cyclone V



Cost Efficiency Space

Arria V



Efficiency Cost

Benchmarking

- Proven performance advantage
- Power, size, noise, cost

Stratix V



Efficiency XCVR noise



Reference Designs Collateral

- User guide and reference manual
- Schematics
- Board Layout
- Gerber files for Board
- Gerber files for individual power components
- Complete BOM list
- Validation data pack
- Full source for test environment



Alignment with FPGA Roadmap





Alignment with FPGA Roadmap

Existing power products

Cost Efficiency Space



Cost Efficiency Space



Efficiency Cost



Efficiency XCVR noise



Other key features Ease of use, TTM, Reliability

Future products





Key power requirements Stratix 10

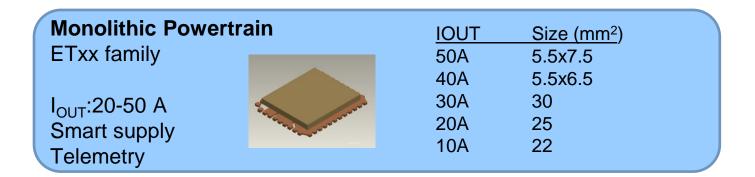
- ➤ Higher Power
- > Tight VOUT voltage tolerance
- ➤ Intelligent voltage control
- ➤ Low noise Transceiver power
- ➤ Comms Bus for control/telemetry
- > Higher current
- ➤ Low profile (<2.5mm for PCle)
- > Performance (efficiency, transient)





What's Next?

Sneak Peak at Power Train and High Current Digital Solution



Integrated Digital Module

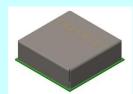
25Mx Family

12V

 $I_{OUT} > 10A$

Bus: SVID/SMBus

Telemetry



<u>IOUT</u>	Size (mm²)
30A	200
20A	170
15A	130
10A	120



Summary

- Altera now offers complete, validated, solutions to our customers; power for FPGA and for all other system blocks to support our customer's requirements.
- Altera's Enpirion Power Solutions provide:
 - Smallest solution size and highest efficiency vs density
 - Low noise and ripple for efficiently powering SERDES and PLL
 - Excellent transient performance
 - Very high reliability
 - And, very easy design for fastest time to market (and revenue for our customers)
- Fully validated reference designs are available in Q4'13 for:
 - Stratix V GX, Arria V GX, Cyclone V GT, Cyclone V SoC
- Altera is in the power business and we are ready now!



Thank You





Product Selector Guide



ENPIRION POWER SOCS lout									Resistor Divider VOUT Set	VID VOUT Set	POK Flag	Programmable Soft Start	Pecision Enable	Input Synchronization	Clock Output	Parallel Capability	Programmable Frequency	Light Load Mode (AB-LLM)	Pre-Bias Startup	Over Voltage Protection	Over Current Protection	Over Temp Protection	Approved for IBC usage	VDDQ Tracking	External Reference	Margining Pin
PN	(A)	(VDC)	(VDC)	(pins)	L	W	Н	Size mm2	Re			Pr					Pr	Lig		0	Ó	J	A			
		STAND	ARD 5V INPU	r Produc	TS																					
EP5348QI							20													•	•					
EP5357xUI	0.6	2.4 - 5.5	0.6 - VIN	uQFN16	2.5	2.25	1.1	14	•	•								•			•	•				
EP5358xUI	0.6	2.4 - 5.5	0.6 - VIN	uQFN16	2.5	2.25	1.1	14	•	•											•	•				
EP5368QI	0.6	2.4 - 5.5	0.6 - VIN	QFN16	3	3	1.1	21	•	•											•	•				
EP5388QI	0.8	2.4 - 5.5	0.6 - VIN	QFN16	3	3	1.1	28	•	•											•	•				
EP53A7xQI	1	2.4 - 5.5	0.6 - VIN	QFN16	3	3	1.1	21	•	•								•			•	•				
EP53A8xQI	1	2.4 - 5.5	0.6 - VIN	QFN16	3	3	1.1	21	•	•											•	•				
EP53F8QI	1.5	2.4 - 5.5	0.6 - VIN	QFN16	3	3	1.1	40	•		•										•	•				
EN5319QI	1.5	2.4 - 5.5	0.6 - VIN	QFN24	4	6	1.1	55	•		•										•	•				
EN5322QI	2	2.4 - 5.5	0.6 - VIN	QFN24	4	6	1.1	58	•	•	•										•	•				
EN5329QI	2	2.4 - 5.5	0.6 - VIN	QFN24	4	6	1.1	55	•		•										•	•				
EN5337QI	3	2.4 - 5.5	0.75 - VIN	QFN38	4	7	1.85	75	•		•	•		•							•	•				
EN5339QI	3	2.4 - 5.5	0.6 - VIN	QFN24	4	6	1.1	55	•		•										•	•				
EN5365/6QI	6	2.4 - 5.5	0.75 - VIN	QFN58	10	12	1.85	229	•	•	•	•				•				•	•	•				\square
EN5367QI	6	2.5 - 5.5	0.75 - VIN	QFN54	5.5	10	3	210	•		•	•		•		•					•	•				Ш
EN5395QI	9	2.4 - 5.5	0.75 - 3.3	QFN58	10	12	1.85	277		•	•					•					•	•				Ш
EN5396QI	9	2.4 - 5.5	0.75 - VIN	QFN58	10	12	1.85	282	•		•					•					•	•				.



Product Selector Guide



POWER SOCS							Resistor Divi	VID VC	POK	Programma	Pecisio	tSync	Clock	Parallel (Programmab	Light Load M	Pre-Bia	Over Voltag	Over Curre	Over Temp	Approvedf	VDDQT	External	Margin			
	lout	Vin	Vo Range	Pkg	Pkg	Size (mm)	Solution	Solution 8			rogr	-	Input		Par	ogra	T T	빏	=	ver	ver	Over	pp	>	EX	
PN	(A)	(VDC)	(VDC)	(pins)	L	W	Н	Size mm²	Size mm² 🛎			=					F	ž		0	0		٩				
6V INPUT PRODUCTS																											
EN5311QI	1	2.4 - 6.6	0.6 - VIN	QFN20	4	5	1.1	36		•											•	•	•				
EN5335/6QI	3	2.4 - 6.6	0.75 - VIN	QFN44	7.5	10	1.85	157	•	•	•	٠								•	•	•	•				
EN6337QI	3	2.4 - 6.6	0.6 - VIN	QFN38	4	7	1.85	75			•	٠		•				•			•	•	•				
EN6347QI	4	2.4 - 6.6	0.6 - VIN	QFN38	4	7	1.85	75			•	•		•				•			•	•	•				
EN5364QI	6	2.4 - 6.6	0.6 - VIN	QFN68	8	11	1.85	160			•		•	•	•	•			•	•	•	•	•			•	
EN6360QI	8	2.4 - 6.6	0.6 - VIN	QFN68	8	11	3	195	•		•		•	•	•	•	•		•		•	•	•				
EN5394QI	9	2.4 - 6.6	0.6 - VIN	QFN68	8	11	1.85	190			•		•	•	•	•			•	•	•	•	•			•	
EN63A0QI	12	2.4 - 6.6	0.6 - VIN	QFN76	10	11	3	227			•		•	•	•	•	•		•		•	•	•				
		12	V INPUT PRO	DUCTS																							
EC2630QI	4	8.0 - 13	4.5 - 6.6	QFN36	5.5	5.5	0.9	140			•			•	•	•	•				•	•	•				
EN2340QI	4	4.5 - 14	0.75 - 5.0	QFN68	8	11	3	200			•	•		•	•	•	•					•					
EN2360QI	6	4.5 - 14	0.60 3.3	QFN68	8	11	3	200			•	٠		•	•	•	•					•					
EN2390QI	9	4.5 - 14	0.60 3.3	QFN76	10	11	3	235			•	•		•	•	•	•					•					
EN23F0QI	15	4.5 - 14	0.60 3.3	QFN92	13	12	3	325			•	٠		•	•	•	•					•					
DDR MEMORY TERMINATION PRODUCTS																											
EV1320QI	3	1 - 1.8	0.5 -0.9	QFN16	3.3	3.3	0.9	40			•	٠				•					•	•		•			
EV1340QI	5	1 - 1.8	0.6 -1.2	QFN54	5.5	10	3	125	•		•	٠				•					•	•		•	•		
EV1380QI	8	1 - 1.8	0.6 -1.2	QFN	8	11	3	200			•	٠				•			•		•	•		•	•		
		CURRENT SEN	ISE AND MONIT	TORING PE	RODUC	CTS		•																			
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Reference

Tracking

p Protection

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